

Customer No.: 31561
Application No.: 10/709,953
Docket No.: 10546-US-PA

AMENDMENTS

Please amend the claims according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

To the Claims:

1. (currently amended) A chip packaging structure, comprising:

a chip having a first passivation layer and at least a bonding pad, wherein the bonding pad is exposed by the first passivation layer and the first passivation layer has at least a recess, the whole recess has a sidewall and a bottom surface being exposed;

a redistribution layer formed over the first passivation layer, wherein the redistribution layer electrically connects with the bonding pad and extends from the bonding pad to the recess, and in contact with the sidewall and the bottom surface of the recess and the redistribution layer further comprises:

a first metallic layer formed over the first passivation layer, wherein a material constituting the first metallic layer is selected from the group consisting of aluminum, titanium, titanium-tungsten alloy, tantalum, tantalum nitride and chromium;

a second metallic layer formed over the first metallic layer; and

a third metallic layer formed over the second metallic layer;

a second passivation layer formed over the first passivation layer and the redistribution layer, wherein the second passivation layer has an opening that exposes the redistribution layer above the recess; and

at least a bump disposed inside the opening and electrically connected to the

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redistribution layer above the recess.

2. (previously presented) The chip packaging structure of claim 1, wherein the recess has an obtuse angle and is formed between the sidewall of the recess and the bottom surface of the recess.

3. (previously presented) The chip packaging structure of claim 1, further comprising at least an under-bump-metallurgy layer formed in the opening of the second passivation layer and extending over an upper surface of the second passivation layer, wherein the bump is on the under-bump-metallurgy layer and electrically connected to the redistribution layer above the recess.

4. (withdrawn) The chip structure of claim 3, wherein the under-bump-metallurgy layer further comprises:

- a first metallic layer formed over the opening-exposed redistribution layer; and
- a second metallic layer formed over the first metallic layer.

5. (withdrawn) The chip structure of claim 4, wherein a material constituting the first metallic layer is selected from the group consisting of aluminum, titanium, titanium-tungsten alloy, tantalum, tantalum nitride and chromium.

6. (withdrawn) The chip structure of claim 4, wherein a material constituting the second metallic layer comprises copper.

7. (withdrawn) The chip structure of claim 4, wherein the under-bump-metallurgy layer further comprises at least an electroplated layer formed over the second metallic layer and the electroplated layer is selected from the group consisting of an electroplated copper layer, an

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electroplated nickel layer, an electroless nickel layer, an electroless plated gold layer and combination thereof.

8. (previously presented) The chip packaging structure of claim 3, wherein the under-bump-metallurgy layer further comprises:

a first metallic layer formed over the opening-exposed redistribution layer;

a second metallic layer formed over the first metallic layer; and

a third metallic layer formed over the second metallic layer.

9. (previously presented) The chip packaging structure of claim 8, wherein a material constituting the first metallic layer is selected from the group consisting of aluminum, titanium, titanium-tungsten alloy, tantalum, tantalum nitride and chromium.

10. (previously presented) The chip packaging structure of claim 8, wherein a material constituting the second metallic layer is selected from the group consisting of nickel-vanadium alloy and copper-chromium alloy.

11. (previously presented) The chip packaging structure of claim 8, wherein a material constituting the third metallic layer comprises copper.

12. (previously presented) The chip packaging structure of claim 8, wherein the under-bump-metallurgy layer further comprises at least an electroplated layer formed over the third metallic layer and the electroplated layer is selected from the group consisting of an electroplated copper layer, an electroplated nickel layer, an electroplated gold layer and combination thereof.

Claims 13-14 (cancelled)

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15. (withdrawn and currently amended) The chip packaging structure of claim 13, wherein a material constituting the second metallic layer comprises copper.

Claims 16-17 (cancelled)

18. (currently amended) ~~The~~ A chip packaging structure of claim 16, comprising:

a chip having a first passivation layer and at least a bonding pad, wherein the bonding pad is exposed by the first passivation layer and the first passivation layer has at least a recess, the whole recess has a sidewall and a bottom surface being exposed;

a redistribution layer formed over the first passivation layer, wherein the redistribution layer electrically connects with the bonding pad and extends from the bonding pad to the recess, and in contact with the sidewall and the bottom surface of the recess and the redistribution layer further comprises:

a first metallic layer formed over the first passivation layer;

a second metallic layer formed over the first metallic layer, wherein a material constituting the second metallic layer is selected from the group consisting of nickel-vanadium alloy and copper-chromium alloy; and

a third metallic layer formed over the second metallic layer;

a second passivation layer formed over the first passivation layer and the redistribution layer, wherein the second passivation layer has an opening that exposes the redistribution layer above the recess; and

at least a bump disposed inside the opening and electrically connected to the redistribution layer above the recess..

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19. (currently amended) The chip packaging structure of claim 186, wherein a material constituting the third metallic layer comprises copper.

20. (previously presented) The chip packaging structure of claim 1, wherein an obtuse angle is formed between a sidewall of the opening and a bottom surface of the opening.

21. (new) The chip packaging structure of claim 18, wherein the recess has an obtuse angle and is formed between the sidewall of the recess and the bottom surface of the recess.

22. (new) The chip packaging structure of claim 18, further comprising at least an under-bump-metallurgy layer formed in the opening of the second passivation layer and extending over an upper surface of the second passivation layer, wherein the bump is on the under-bump-metallurgy layer and electrically connected to the redistribution layer above the recess.